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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/653,889	09/04/2003	Makoto Yoshida	501.37959CC2	4939
20457	7590	08/10/2004	EXAMINER	
ANTONELLI, TERRY, STOUT & KRAUS, LLP 1300 NORTH SEVENTEENTH STREET SUITE 1800 ARLINGTON, VA 22209-9889			PHAM, HOAI V	
			ART UNIT	PAPER NUMBER
			2814	

DATE MAILED: 08/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/653,889	Applicant(s) YOSHIDA ET AL.	
	Examiner Hoai v Pham	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 June 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 11-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 11-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>09/04/03</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 11-13 and new claims 14-16 in the reply filed on June 14, 2004 is acknowledged.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.
4. Claims 11-16 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.
5. Claims 11 and 14, lines 15-16, the phrase "a diameter of said first opening is less than that of said second opening and such that said second opening reaches said semiconductor regions" is not enabled because the specification

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and the drawing shown that the diameter of said first opening is larger than the second opening.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 11-16, insofar as clear, are rejected under 35 U.S.C. 102(e) as being anticipated by Kasai et al. [U.S. Patent 6,448,597].

With respect to claim 11, Kasai et al. (figs. 14A-14F, cols. 5-9] discloses a semiconductor integrated circuit device, comprising:

a semiconductor substrate (12) with an active region defined by an element isolation region (13), word lines (14) extending in a first direction over said active region such that gate electrodes (34) of metal insulator semiconductor field effect transistors (MISFETS) are electrically coupled to said word lines (14), semiconductor regions formed in said active region such that said semiconductor regions (36) serve as a source region or a drain region of each MISFET;

a first insulating film (71A) covering said active region, said word lines (14) and said semiconductor regions (36);

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a first opening (79) formed in said first insulating film such that said first opening is arranged between said word lines and extends, in said first direction, from a semiconductor region to said element isolation region (13);

a second opening (79) formed in said first insulating film under said first opening such that, in said first direction, a diameter of said first opening is larger than that of said second opening and such that said second opening reaches said semiconductor regions;

a conductive material (74) buried in said first opening and in said second opening; and

a bit line (38) formed over said first insulating film such that said bit line is electrically coupled to said conductive material (34) and extends to cross said word lines (see fig. 8).

With respect to claim 12, Kasai et al. further discloses:

a capacitor element (52) formed over said first insulating film (71A);

a third opening (79) formed in said first insulating film (71A) to reach other semiconductor region (36); and

a conductive material (74) buried in said third opening (79),

wherein said capacitor element (52) is electrically coupled to the other semiconductor region (36) through said conductive material (74) buried in said third opening (79) (see fig. 14F and col. 8, lines 64-67).

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With respect to claim 13, Kasai et al. discloses that a memory cell of a dynamic random access memory is comprised of said MISFET (14) and said capacitor element (52) (see the Abstract).

With respect to claim 14, Kasai et al. (figs. 14A-14F, cols. 5-9] discloses a semiconductor integrated circuit device, comprising:

a semiconductor substrate (12) with an active region defined by an element isolation region (13), word lines (14) extending in a first direction over said active region such that gate electrodes (34) of metal insulator semiconductor field effect transistors (MISFETS) are electrically coupled to said word lines (14), semiconductor regions formed in said active region such that said semiconductor regions (36) serve as a source region or a drain region of each MISFET;

a first insulating film (71A) covering said active region, said word lines (14) and said semiconductor regions (36);

a first opening (79) formed in said first insulating film such that said first opening is arranged between said word lines and extends, in said first direction, from a semiconductor region to said element isolation region (13);

a second opening (79) formed in said first insulating film under said first opening such that, in said first direction, a diameter of said first opening is larger than that of said second opening and such that said second opening reaches said semiconductor regions;

a third opening (79) formed in said first insulating film (71A) to reach other semiconductor region (36);

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a conductive material (74) buried in said first opening and in said second opening; and

a bit line (38) formed over said first insulating film such that said bit line is electrically coupled to said conductive material (34) and extends to cross said word lines (see fig. 8].

With respect to claim 15, Kasai et al. further discloses:

a capacitor element (52) formed over said first insulating film (71A),
wherein said capacitor element (52) is electrically coupled to the other semiconductor region (36) through said conductive material (74) buried in said third opening (79) (see fig. 14F and col. 8, lines 64-67).

With respect to claim 16, Kasai et al. discloses that a memory cell of a dynamic random access memory is comprised of said MISFET (14) and said capacitor element (52) (see the Abstract).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoai v Pham whose telephone number is 571-272-1715. The examiner can normally be reached on M-F.

9. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M Fahmy can be reached on 571-272-1705. The

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fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'Hoai Pham', with a long horizontal flourish extending to the right.

Hoai Pham
Patent Examiner